ABSTRACT

A phase detector and signal locking system controller for use in a digital phase-locked loop (PLL) application includes a first and a second phase detector where the first phase detector result is used to control the initial pull-in and the second phase detector is used to control fine tuning once the phase differences are too small for appropriate detection by the first phase detector. A post processing and control unit operates to effectively merge the two phase detector outputs and to apply the appropriate gain factor that can be used to control a PLL system.